Patent
Attorney's Docket No. 040050-050

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
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Karl-Magnus MÖLLER	)	
	)	
Application No.: UNASSIGNED	)	Group Art Unit: UNASSIGNED
	)	
Filed: December 21, 2001	)	Examiner: UNASSIGNED
	)	
For: DIGITAL BUS SYSTEM	)	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 1 - 12 as follows:

1. (Amended) A digital bus system comprising:
at least one first data bus that includes at least one data line;
a plurality of transmitter units that are connected to the first data bus;
at least one receiver that is connected to the first data bus;
means for generating a clock signal which indicates the rate at which data is sent on the first data bus; and
means for distributing the clock signal to the transmitter units, characterized in that
the bus system includes means for establishing at least one first parameter that indicates the number of transmitter units which have a need to send data over said first data bus; and in that
said clock signal generating means are adapted to generate the clock signal in relation to at least the first parameter in accordance with a predetermined pattern, so that the data rate on

the first data bus will decrease in response to a reduction in the number of transmitter units that need to send data over the first data bus.

2. (Amended) A digital bus system according to Claim 1, wherein the means for generating the clock signal include:
means for generating a reference signal that has a predetermined frequency;
frequency modifying means adapted to receive the reference signal and to generate the clock signal by frequency modifying said reference signal; and
control means for controlling said frequency modification in relation to the first parameter.

3. (Amended) A digital bus system according to Claim 2, wherein the frequency modifying means include a controllable frequency divider.

4. (Amended) A digital bus system according to Claim 3, wherein the frequency divider includes:
a binary counter that has a predetermined number of bits, said binary counter being adapted to receive the reference signal; and
a controllable selector, which is connected to the binary counter and adapted to select one of the bits from the counter in response to the control from the control means, wherewith the bit selected constitutes the clock signal.

5. (Amended) A digital bus system according to Claim 1, wherein the means for generating the clock signal include a digitally controlled oscillator.

6. (Amended) A digital bus system according to Claim 1, wherein the transmitter units include means for requesting permission to send data over the first data bus.

7. (Amended) A digital bus system according to Claim 6, wherein the bus system further includes means for establishing the number of requesting transmitter units, and wherein the

means for establishing the first parameter are adapted to establish said first parameter on the basis of the established number of requesting transmitter units.

8. (Amended) A digital bus system according to Claim 6, wherein the bus system further includes:
means or determining and controlling the order in which the requesting transmitter units send data over the first data bus.

9. (Amended) A digital bus system according to Claim 7, wherein the bus system is adapted to switch off the clock signal when the established number of requesting transmitter units is zero.

10. (Amended) A digital bus system according to Claim 1, wherein the transmitter units include means for detecting collisions on the first data bus.

11. (Amended) A digital bus system according to Claim 10, wherein the bus system includes means for establishing at least a first value that indicates the collision intensity on the first data bus, and wherein the means for establishing the first parameter are adapted to establish said first parameter on the basis of said first value.

12. (Amended) A digital bus system according to Claim 11, wherein said first value corresponds to the number of transmitter units that have newly detected a collision.

REMARKS

The claims of the originally-filed application were drafted in accordance with a foreign patent practice. The claims are hereby amended merely to present an initial set of claims for examination that conform to U.S. patent practice.

Respectfully submitted,

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Date: December 21, 2001

Attachment to Preliminary Amendment dated December 21, 2001

Marked-up claims 1-12

1. (Amended) A digital bus system [(1; 1a)] comprising:
at least one first data bus [(3)] that includes at least one data line [(3b)];
a plurality of transmitter units [(9.1-9.N)] that are connected to the first data bus;
at least one receiver [(15)] that is connected to the first data bus;
means [(5; 5a)] for generating a clock signal [(CLK2)] which indicates the rate at which data is sent on the first data bus; and
means [(3a)] for distributing the clock signal to the transmitter units, [characterised] characterized in that
the bus system includes means [(25, 31)] for establishing at least one first parameter [(M; M1)] that indicates the number of transmitter units which have a need to send data over said first data bus; and in that
said clock signal generating means are adapted to generate the clock signal in relation to at least the first parameter in accordance with a predetermined pattern, so that the data rate on the first data bus will decrease in response to a reduction in the number of transmitter units that need to send data over the first data bus.

2. (Amended) A digital bus system [(1; 1a)] according to Claim 1, wherein the means [(5; 5a)] for generating the clock signal [(CLK2)] include:
means [(33)] for generating a reference signal [(34)] that has a predetermined frequency;
frequency modifying means adapted to receive the reference signal and to generate the clock signal by frequency modifying said reference signal; and
control means [(39)] for controlling said frequency modification in relation to the first parameter [(M; M1)].

3. (Amended) A digital bus system [(1; 1a)] according to Claim 2, wherein the frequency modifying means include a controllable frequency divider.

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Marked-up claims 1-12

4. (Amended) A digital bus system according to Claim 3, wherein the frequency divider includes:
a binary counter [(35)] that has a predetermined number of bits, said binary counter being adapted to receive the reference signal [(34)]; and
a controllable selector [(37)], which is connected to the binary counter and adapted to select one of the bits from the counter in response to the control from the control means [(39)], wherewith the bit selected constitutes the clock signal [(CLK2)].

5. (Amended) A digital bus system [(1; 1a)] according to Claim 1, wherein the means for generating the clock signal [(CLK2)] include a digitally controlled oscillator [(37)].

6. (Amended) A digital bus system [(1)] according to [any one of Claims 1 to 5 inclusive] Claim 1, wherein the transmitter units [(9.1-9.N)] include means [(11.1-11.N)] for requesting permission to send data over the first data bus [(3)].

7. (Amended) A digital bus system [(1)] according to Claim 6, wherein the bus system further includes means [(25, 31)] for establishing the number of requesting transmitter units [(9.1-9.N)], and wherein the means for establishing the first parameter are adapted to establish said first parameter on the basis of the established number of requesting transmitter units.

8. (Amended) A digital bus system according to [any one of Claims 6 or 7] Claim 6, wherein the bus system further includes:
means [(27, 29, 7)] for determining and controlling the order in which the requesting transmitter units [(9.1-9.N)] send data over the first data bus [(3)].

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Marked-up claims 1-12

9. (Amended) A digital bus system [(1)] according to [any one of Claims 7 or 8] Claim 7, wherein the bus system is adapted to switch off the clock signal [(CLK2)] when the established number of requesting transmitter units [(9.1-9.N)] is zero.

10. (Amended) A digital bus system [(1a)] according to [any one of Claims 1 to 5 inclusive] Claim 1, wherein the transmitter units [(9.1-9.N)] include means for detecting collisions on the first data bus [(3)].

11. (Amended) A digital bus system [(1a)] according to Claim 10, wherein the bus system includes means [(13.1a-13.Na, 7.1, 25, 31)] for establishing at least a first value [(M1)] that indicates the collision intensity on the first data bus [(3)], and wherein the means for establishing the first parameter are adapted to establish said first parameter on the basis of said first value.

12. (Amended) A digital bus system [(1a)] according to Claim 11, wherein said first value [(M1)] corresponds to the number of transmitter units [(9.1-9.N)] that have newly detected a collision.